IN THE SPECIFICATION:

Please amend the specification at paragraph [00113] as follows:

--Another method for determining whether a physical description falls within a tolerance region is illustrated in Figures 17a and~~-17bb~~ 17b. Associated with target wafer shape (1711) are two tolerance surfaces: a minimum tolerance surface (1712) and a maximum tolerance surface (1713). We can perceive the tolerance region associated with the target wafer shape (1711) as the volume between the minimum and maximum tolerance surfaces. Manufacturing check can then proceed by evaluating whether the physical description (1714) encloses the minimum tolerance surface (1712) and whether the maximum tolerance surface (1713) encloses the physical description (1714). Simultaneous fulfillment of both criteria indicates passing of manufacturing check. In the special case where the tolerance region is a two-dimensional surface, the tolerance surfaces become curves.--

Please amend the specification at paragraph [00114] as follows:

--Besides manufacturing check, electrical check (1214) expressed in FIG. 12 can be implemented using the unified model according to the example shown in FIG. 18a-18c. The layout shown in ~~FIGS. 18a-a-~~FIG. 18a is a part of a complementary metal-oxide silicon (CMOS) inverter. It comprises three shapes (1801), (1802), and (1803). Rectangles (1801) and (1802) are the transistor active areas for the p-type and n-type transistors. Shape (1803) belongs to the polysilicon level. Intersections of polysilicon and active area form the transistor gates. A decomposition of the layout can result in the shapes shown in FIGS. 18a~~-b~~ and 18b, where shape (1803) is decomposed into three rectangles (1804), (1805), and (1806). (Note that decomposition of the layout for electrical check may be different from the decomposition for manufacturing check.) The rectangles (1801) and (1802) are intact. The shapes of the decomposed layout are then identified with circuit elements. Three circuit elements can be identified from the decomposed layout shown in ~~FIGS. 18a-b~~FIG. 18b: a first transistor comprising shapes (1801) and (1805), a second transistor comprising shapes (1802) and (1806), and a conductor (1804). Let us focus on electrical check of the second transistor consisting of shapes (1802) and (1806). In general electrical check verifies many properties of the circuit elements. To illustrate the principle, the check will be restricted to leakage current verification, with the requirement that the transistor leakage current must be less than the maximum allowable leakage current $I_{leakage,max}$. The value of $I_{leakage,max}$ can be derived from the electrical parameters of the unified model. Applying the unified model on the decomposed shapes (1802) and (1806) gives their three-dimensional physical descriptions (1807) and (1808), as shown in ~~FIGS. 18a-c~~FIG. 18c. Transistor parameters can then be determined from these physical descriptions. With these parameters, a CMOS parametric representation within the unified model can compute the leakage current $I_{leakage,max}$. In the case that $I_{leakage}$ is larger than $I_{leakage,max}$, electrical check fails. This failure and the location of the circuit element constitute part of the decision and output data of layout verification.--